Journal of the Korean Physical Society, Vol. 45, No. 5, November 2004, pp. 1384∼1390

Two-Dimensional Quantum Effects and Structural Optimization of FinFETs with Two-Dimensional Poisson-Schrödinger Solver

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(Received 7 July 2004)

In this paper, we present our numerical study on the short-channel performance of a FinFET. Our theoretical work is based on the solution of the Poisson-Schrödinger equations in a self-consistent manner. The calculated current-voltage (I-V) characteristics from our two-dimensional solver were compared with experimental data. To suppress the short-channel effects of a nanometer-scale FinFET, the structural dimensions such as the Si-fin thickness (T_{fin}) and the gate length (L_g) were optimized in terms of subthreshold swing, threshold-voltage roll-off, and drain-induced barrier lowering as well as the transconductance. Quantum-confinement effects for the electron density were also examined by varying T_{fin}.

PACS numbers: 85.30.De
Keywords: FinFET, Quantum-mechanical simulation, Short-channel effects, Coupled poisson-schrödinger equations, Quantum effects

I. INTRODUCTION

Recently, a double-gate (DG) structure has attracted a great deal of attention for its potential to be applied to sub-40 nm MOSFETs. Among the many versions of DG MOSFETs, a self-aligned DG MOSFET structure, a so-called FinFET, is one of the most promising candidates for the implementation of a nano-scale planar MOSFET [1–5]. In order to optimize the structure of a FinFET, it is necessary to undertake a two-dimensional (2-D) quantum-mechanical (QM) simulation, due to its inherent quantum effects on the electronic properties in the nano-scale regime. To fulfill the numerical simulation of nano-scale structures such as FinFET, we need to obtain a self-consistent solution of the coupled Poisson-Schrödinger equations.

In this paper, we report our self-consistent QM approach for the analysis of FinFETs. The electrical performance of FinFETs was carefully investigated in terms of channel length (L_g) (10 ∼ 80 nm) and Si-fin thickness (T_{fin}) (5 ∼ 75 nm). Structural optimizations were performed in order to suppress the short-channel effects (SCE) and simultaneously to increase transconductance (G_m). Some critical parameters such as subthreshold swing, threshold-voltage (V_t) roll-off and drain-induced barrier lowering (DIBL) were examined. At the same time, the differences between the classical and QM simulation results and especially quantum effects were examined in terms of I-V characteristics and electron densities.

II. NUMERICAL MODEL

The 2-D QM model for obtaining the band structure is based on the self-consistent solution of coupled Poisson-Schrödinger equations:

$$\nabla \cdot [\epsilon(x,y)\nabla\Phi(x,y)] = -\rho(x,y), \tag{1}$$

$$\rho(x,y) = q[-n(x,y) + p(x,y) + N_D^+(x,y) - N_A^-(x,y)], \tag{2}$$

$$-\frac{h^2}{2}\nabla \cdot \left[\frac{1}{m^*}\nabla\Psi_n(x,y)\right] + V(x,y)\Psi_n(x,y) = E_n\Psi_n(x,y), \tag{3}$$

where ϵ is the dielectric constant, Φ the electrostatic potential, ρ the total charge density, n and p the electron and hole concentrations, N_D^+ and N_A^- the ionized donor and acceptor concentrations, $\Psi_n(x,y)$ the wave function of nth eigenstates, η Planck's constant divided by 2π,

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$m^*(x,y)$ the effective mass, E_n the energy of nth eigenstates, and V the potential energy, which is given by $V(x,y) = \Delta E_c(x,y) - q\Phi(x,y)$. Here, $\Delta E_c(x,y)$ is the band offset in the conduction band.

The mixed Dirichlet and von Neumann boundary conditions are used for the Schrödinger equation, because pure Dirichlet boundary conditions force the density to decrease down to zero at contacts while the density increases for the von Neumann boundary conditions. For these reasons, we solve the Schrödinger equation with Dirichlet and Neumann boundary conditions respectively, and normalize the states to 1/2. The mixed Dirichlet and von Neumann boundary conditions are given by the following equation:

$$\int |\Psi(z)|^2 dz = 1/2. \quad (4)$$

This means that we obtain a constant function by summing cosine functions from Dirichlet boundary conditions and sine functions from von Neumann boundary conditions with normalization to 1/2.

By solving the Schrödinger equation, we obtain the quantized states which are occupied with the local quasi-Fermi levels. The 2-D quantum electron density is found by using

$$n(x,y) = \frac{1}{\pi\eta}\sqrt{2m^* k_B T}\sum_j |\Psi_j(x,y)|^2 \times F_{-1/2}\left(\frac{E_F - E_j}{k_B T}\right), \quad (5)$$

where E_j and $\Psi_j(x,y)$ are the energy and the wave function of the jth eigenstate, $E_F(x,y)$ the Fermi level, and F_k the Fermi-Dirac integrals of order k. These integrals are defined as follows:

$$F_k(\eta) = \frac{1}{\Gamma(k+1)}\int_0^\infty \frac{u^k du}{1+e^{u-\eta}}, \quad k \geq -1, \quad (6)$$

and also have the following property:

$$\frac{d}{d\eta}F_k(\eta) = F_{k-1}(\eta), \quad k \leq -1. \quad (7)$$

We obtain the semi-classical current solution from the 1st moment of the Boltzmann equation by adopting a simple drift-diffusion model for the electron current:

$$J_n(x,y) = \mu_n(x,y) n(x,y) \nabla E_{Fn}(x,y). \quad (8)$$

The continuity Equation for current density is given by

$$\nabla \cdot J_n(x,y) = -R(x,y). \quad (9)$$

As per a model of carrier mobility, a physics-based and semi-empirical model was employed for the wide range of channel doping, electric field, and temperature. To take various scattering mechanisms into account, the Mathiessen rule was applied in order to fully consider a specific scattering mechanism extracted from experimental data as a function of doping concentration, electric field, and temperature for carrier mobility in the channel [6].

$$\frac{1}{\mu} = \frac{1}{\mu_b} + \frac{1}{\mu_{ac}} + \frac{1}{\mu_{sr}}, \quad (10)$$

where μ_b is the carrier mobility in bulk, μ_{ac} the carrier mobility from the surface acoustic phonon scattering, and μ_{sr} the carrier mobility from surface roughness scattering.

The bulk mobility, μ_b, uses the empirical model expressed by Masetti *et al.* [7] which depends on the impurity concentration and temperature.

$$\mu_b(N_A,T) = \mu_0 + \frac{\mu_{max}(T) - \mu_0}{1 + (N_A/C_r)^\alpha} - \frac{\mu_1}{1 + (C_s/N_A)^\beta}, \quad (11)$$

$$\mu_{max}(T) = \mu_{max}\left(\frac{T}{300}\right)^{-\gamma}, \quad (12)$$

where N_A is the local acceptor concentration, and γ_{init} = 2.42, the initial estimate for γ.

The electron mobility for the acoustic phonon scattering and nondegenerate surface, μ_{ac}, is expressed by [6]

$$\mu_{ac}(E_\perp, T) = \left(\frac{BT}{E_\perp} + \frac{C}{E_\perp^{1/3}}\right)\frac{1}{T}, \quad (13)$$

where $E_\perp$ is the perpendicular electric field to the direction of current flow. Further, B and C are fitting parameters with initial values of $B_{init} = 3.1 \times 10^8$ cm/s and $C_{init} = 3.0 \times 10^7$ (V/cm)$^{-2/3}$·K·cm/s based on physical quantities such as deformation potential, mass density of silicon, and effective thickness of inversion layer [8].

At very high perpendicular electric field, surface roughness scattering, μ_{sr} significantly affects the inversion layer mobility. It is described as follows [6]:

$$\mu_{sr}(E_\perp) = \frac{\delta}{E_\perp^2}, \quad (14)$$

where δ is a constant depending on the oxide growth condition, and the initial value of δ is $\delta_{init} = 6 \times 10^{14}$ V/s.

For the above carrier mobility model, we have arranged the optimized results for the model fitting parameters in Table 1 for electrons and holes.

In order to obtain self-consistent QM solutions, we have employed an iterative procedure [9]. We start out by calculating the electric potential. Next, the program calculates a charge distribution by using an iteration scheme. Thereafter, the program determines self-consistent solutions of Poisson-Schrödinger and current equations [9]. The Newton method has been employed with a constraint that should satisfy error criteria as outlined in [3].

Figure 1 shows a schematic top view of the cross section of the FinFET modeled in this work. Two metal

Table 1. Mobility model parameters.

Parameter	Electrons	Holes	Units
μ_0	52.2	44.9	cm^2/Vs
μ_{max}	1417	470.5	cm^2/Vs
μ_1	43.4	29.0	cm^2/Vs
C_r	9.68×10^{16}	2.23×10^{17}	cm^{-3}
C_s	3.43×10^{20}	6.10×10^{20}	cm^{-3}
α	0.680	0.719	-
β	2.00	2.00	-
γ	2.5	2.2	-
B	4.75×10^7	9.93×10^7	cm/s
C	$1.74 \times 10^5 \times N_A^{0.125}$	$8.84 \times 10^5 \times N_D^{0.125}$	N_A in cm^{-3}
δ	5.82×10^{14}	2.05×10^{14}	-

From Ref. [7]

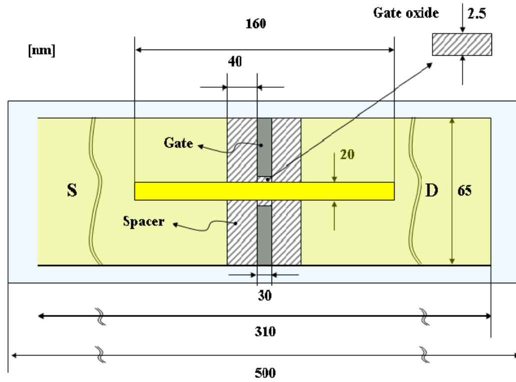

Fig. 1. Schematic diagram illustrating the top view of the cross section of the FinFET used in this study.

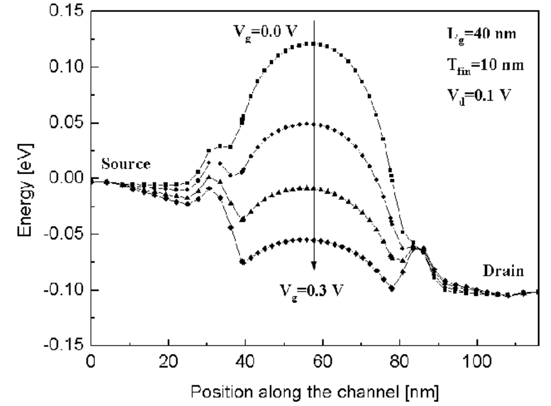

Fig. 2. Conduction-band profiles from source to drain for L_g = 40 nm, T_{fin} = 10 nm, V_d = 0.1 V and V_g = 0.0 ∼ 0.3 V.

gates with gate length L_g and work function Φ_M = 4.1 eV are located symmetrically on both sides of the silicon fin. The source and drain regions are modeled as ohmic contacts with a doping of $1 \times 10^{20}/cm^3$, and under the gate doping is $1 \times 10^{15}/cm^3$. The oxide thickness (T_{ox}) is 2.5 nm, and L_g varies from 10 nm to 80 nm. As a test vehicle for verifying the validity of our numerical simulation, we chose an n-channel FinFET because of its good short-channel performance down to sub-10 nm MOSFETs.

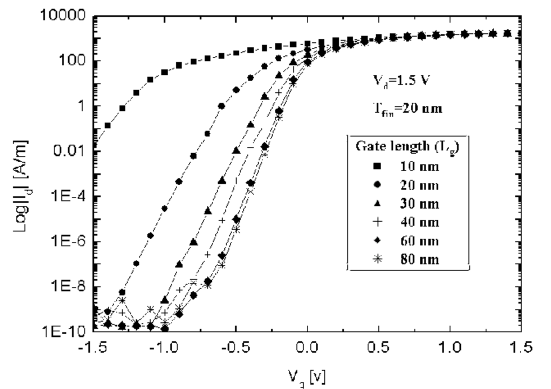

Fig. 3. I_d-V_g curves for n-channel FinFETs with L_g of 10 ∼ 80 nm and T_{fin} = 20 nm.

III. SIMULATION RESULTS

In this work, we estimated the SCE of FinFETs and optimized G_m by performing the simulations for different L_g and T_{fin}. Figure 2 shows conduction-band profiles from source to drain, which are performed under the conditions of L_g = 40 nm, T_{fin} = 10 nm, V_d = 0.1 V and V_g varying from 0.0 V to 0.3 V. The peak value of the conduction band is adjusted by the variation of the gate-voltage variation. Figures 3 and 4 demonstrate the I_d-V_g curves for n-channel FinFETs for different devices. From these figures, we can see clearly that a FinFET with thinner T_{fin} and shorter L_g shows better device characteristics than thicker and longer ones.

To analyze the SCE, we extracted some parameters

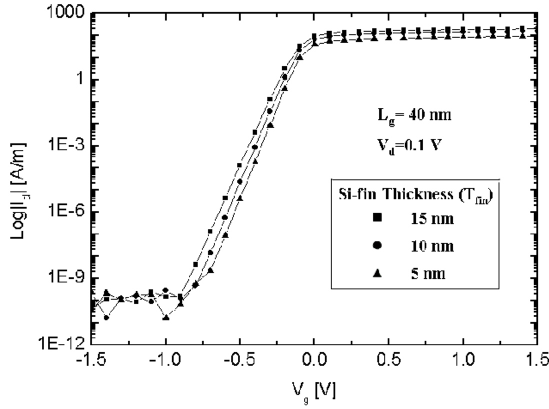

Fig. 4. I_d-V_g curves for n-channel FinFETs with T_{fin} of 5 ∼ 15 nm and L_g = 40 nm.

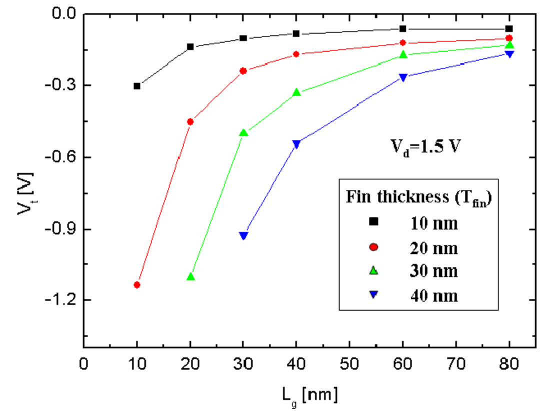

Fig. 6. V_t roll-off of n-channel FinFETs in terms of L_g for different T_{fin}.

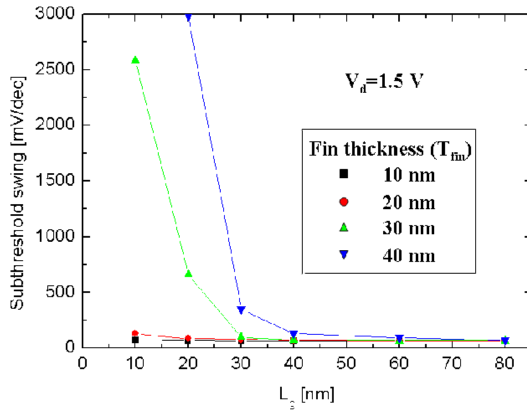

Fig. 5. Subthreshold swing of n-channel FinFETs in terms of L_g for different T_{fin}.

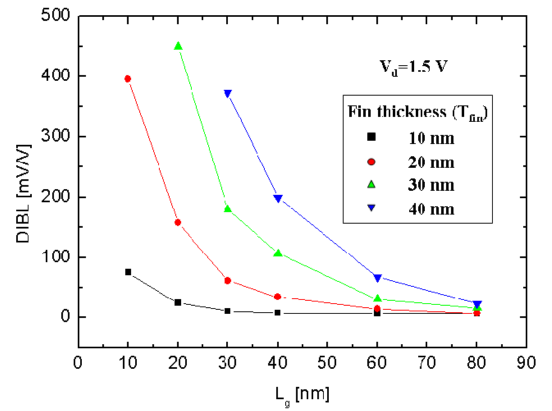

Fig. 7. DIBL characteristics of n-channel FinFETs as a function of L_g.

of subthreshold swing, V_t roll-off and DIBL. Figure 5 demonstrates the subthreshold swings for an n-channel FinFET as a function of L_g for different T_{fin}. In this work, we performed simulations with L_g varying from 10 nm to 80 nm and T_{fin} varying from 10 nm to 40 nm. The simulation results for T_{fin} = 10 nm and 20 nm at V_d = 1.5 V exhibit good SCE. Figure 6 demonstrates the V_t roll-off characteristic under the same condition as Figure 5. The numerical simulation results also show good SCE at smaller T_{fin}. Figure 7 shows the DIBL, which is performed under the same conditions as those of Figure 5. The strength of the DIBL is measured from the difference of V_t as drain voltage changes from 0.1 V to 1.5 V in order to find smaller values than 10 mV/V and to control the devices over wide ranges of L_g.

Figures 8 and 9 show the functional dependence of G_m on T_{fin} and L_g at V_d = 0.05 V and 1.5 V, respectively. Each simulation result reveals that G_m increases as T_{fin} and L_g increase. However, the value of G_m is found to peak at T_{fin} = 65 nm and L_g = 60 nm. The reason for this is that as long as thicker T_{fin} and longer L_g increase the parasitic resistance, the carrier mobility is increased as well. However, the charge centroid is reduced at the

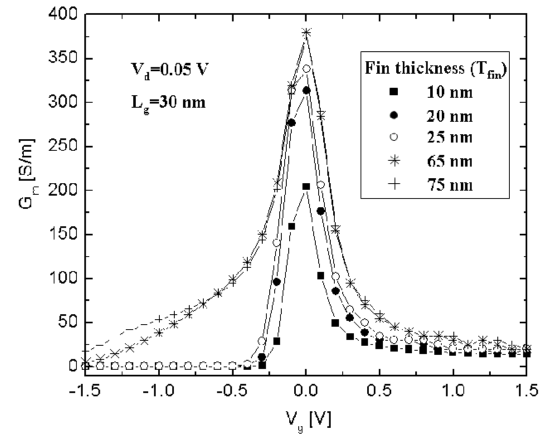

Fig. 8. Dependence of G_m on T_{fin}. G_{mmax} = 380 [S/m] at T_{fin} = 65 nm, and G_{mmax} = 375 [S/m] at T_{fin} = 75 nm.

same time. Consequently, we can obtain the optimal L_g and T_{fins}. To verify the validity of our simulation, we compared our calculations with the experimental results reported in the literature [5]. Figure 10 shows the comparison of the I_d-V_g characteristics for a FinFET with

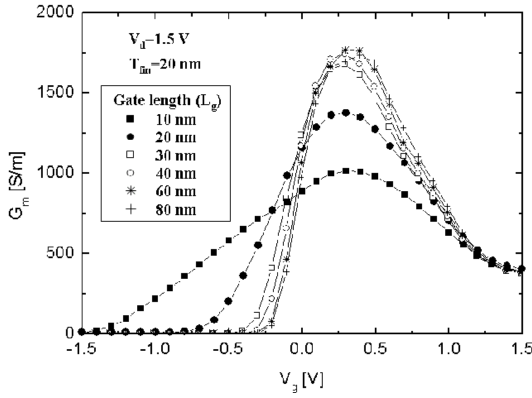

Fig. 9. Dependence of G_m on L_g. G_{mmax} = 1760 [S/m] at L_g = 60 nm, and G_{mmax} = 1689 [S/m] at L_g = 80 nm.

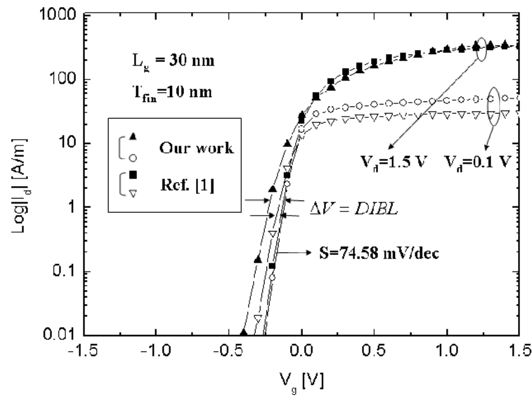

Fig. 10. I_d-V_g curves for a simulated n-channel FinFET with L_g = 30 nm, T_{fin} = 20 nm, compared to experimental data.

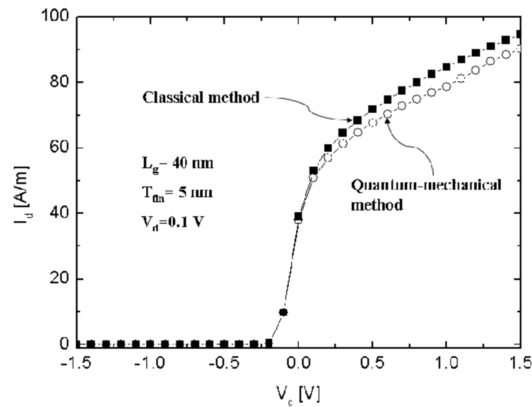

Fig. 11. Difference in the simulation results (I_d-V_g curves) with QM and classical methods.

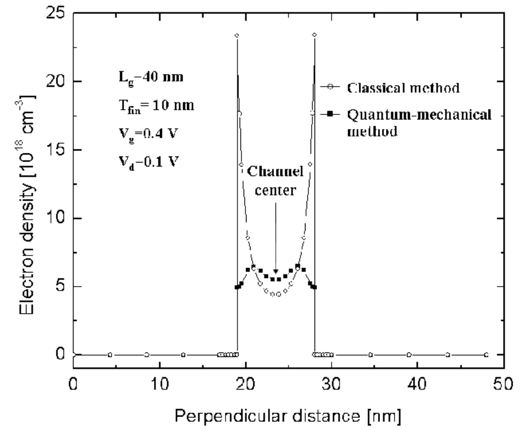

Fig. 12. Comparison of the classical and QM electron density for a cut through the Si channel.

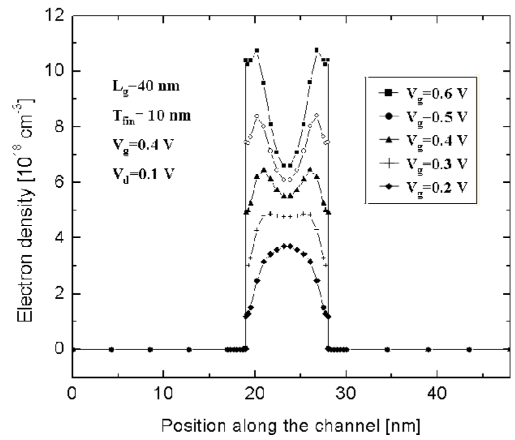

Fig. 13. Cross section of the QM electron density for L_g = 40 nm, T_{fin} = 10 nm, and V_d = 0.1 V at V_g = 0.2 ~ 0.6 V.

L_g = 30 nm, T_{fin} = 20 nm and V_d = 0.1 V and 1.5 V, respectively. The calculated value of the subthreshold swing is 74.6 mV/dec at V_d = 1.5 V. In spite of the low channel doping concentration (phosphorus = 1 × 10^{15} cm^{-3}), the subthreshold leakage current is well suppressed. The subthreshold leakage current is one of the most important factors for the nano-scale semiconductor devices such as the FinFET type. Therefore, an accurate model for the subthreshold leakage current is very crucial for the low-voltage device. However, the effect of impact ionization has not been considered, despite the great effort regarding the subthreshold leakage current for DG MOSFET structure. In this work, we considered the leakage current from impact ionization and thermionic emission. The subthreshold leakage current caused by the impact ionization in the high-electric field region can be modeled by the channel carrier concentration (n_{ch}), effective channel length (L_{eff}), and the coefficient (α_I) which is related with the electric field (E) in the channel. It is as follows [10]:

$$|I_{leakage}| = I_D \cdot L_{eff} \cdot \alpha_I \cong I_D \cdot L_{eff} \cdot \alpha_0 \cdot \exp\left[\frac{-E_0}{E}\right], \quad (15)$$

$$I_D = q \cdot W \cdot n_{ch} \cdot \nu_{eff}, \quad (16)$$

where E_0 is the reference electric field, W the gate width,

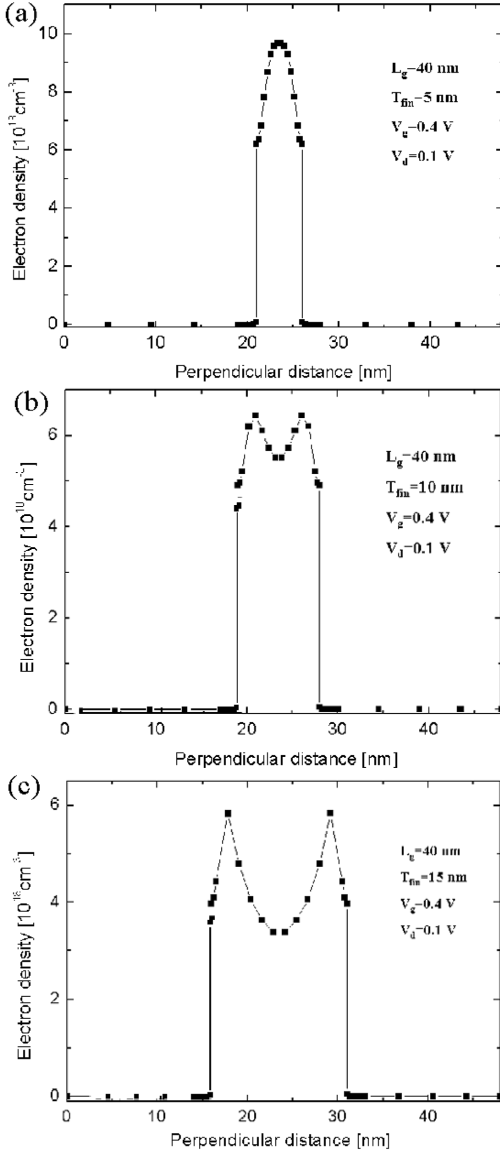

Fig. 14. Cross section of the QM electron density for L_g = 40 nm, T_{fin} = 10 nm, V_g = 0.4 V, and V_d = 0.1 V for T_{fin} equal to (a) 5 nm, (b) 10 nm, and (c) 15 nm.

and ν_{eff} the effective drift velocity. We also note that the reverse leakage current is formed by electron-hole pairs in the high-field region and drift-diffusion component of minority carriers in the depletion region. The reverse leakage current is also strongly related with the Schottky barrier height and significantly increases at large reverse gate bias, due to the thermionic emission and tunneling from the gate to the channel. For the structure of DG-SOI MOSFETs including FinFET, the application of impact ionization and thermionic emission is very important because the electron-hole pairs caused by impact ionization are generated while most of the electrons flow through the center of the bulk and these carriers affect the determination of potential in the bulk. Also, impact ionization can be dominantly influenced by T_{fin}, while thinner T_{fin} is able to suppress effectively the subthreshold leakage current due to the injection of holes in the high-field drain region [11].

Finally, we compared differences in the simulation results for classical and QM simulations. Figure 11 shows the differences in the I_d-V_g characteristics for the two approaches. Here, we find that for the QM simulation the current is suppressed compared to the classical one, due to the quantum-confinement effects. A comparison of the classical and QM electron density as seen for a cut through the Si channel is shown in Figure 12, and QM electron-density variations by changing V_g from 0.2 V to 0.6 V are shown in Figure 13. For a sufficiently thin layer, the peak of QM electron density is located further away from the Si/SiO_2 interface, in comparison with the classical density. The reason for this repulsion of the quantum density from the Si/SiO_2 interface lies directly in the wave nature of the inversion-layer carriers, which are all located in quantized sub-bands [12]. Figures 14(a), (b), and (c) demonstrate the distribution of electrons for several T_{fin}: (a) T_{fin} = 5 nm, (b) T_{fin} = 10 nm, and (c) T_{fin} = 15 nm. These simulations performed under conditions of L_g = 40 nm, V_g = 0.4 V, V_d = 0.1 V exhibit clearly the quantum repulsion discussed earlier, as the peak of electron density is located farther from the Si/SiO_2 interface as the silicon channel becomes thinner. From these results, we can confirm that the inclusion of QM size quantization effects is crucial for the accurate simulation of narrow-channel structures, especially with respect to I-V characteristics and the electron density near the oxide interface.

IV. CONCLUSION

In this paper, we report our 2-D numerical modeling and simulation results for nano-scale FinFETs, together with a comparison with the experimental data. The simulation reveals that short-channel effects can be appreciably suppressed by optimizing the structure of the FinFET with respect to the influence of L_g and T_{fin} on G_m. Quantum effects for thin layers are investigated for the electron density by varying T_{fin} and by comparing the simulation results for classical and QM simulation. Our simulation results imply that the FinFET structure is a promising candidate for implementing sub-30 nm MOSFETs. Our results also show that a self-consistent solution of the coupled Poisson-Schrödinger equations is mandatory in order to accurately analyze nano-scale structures such as FinFETs.

ACKNOWLEDGMENTS

This work was supported partly by the Korean Ministry of Information & Communication (MIC) through

the Information Technology Research Center (ITRC) Program supervised by IITA, and partly by the Korean Ministry of Science and Technology (MOST) through the Tera-Nano Development (TND) Program and the Nano Core Basic Research Program (M1-0213-04-0002) by KISTEP.

REFERENCES

[1] D. Hisamoto, W. C. Lee, J. Kedzierski, H. Takeuchi, K. Asano, C. Kuo, E. Anderson, T. J. King, J. Bokor and C. Hu, IEEE Trans. Electron Devices **47**, 2320 (2000).

[2] A. Svizhenko, M. P. Anantram, T. R. Govindan and B. Biegel, J. Appl. Phys. **91**, 2343 (2002).

[3] S. E. Laux, A. Kumar and M. V. Fischetti, Tech. Dig., International Electron Devices Meeting (2002), p. 715.

[4] I. H. Cho, B. G. Park, J. D. Lee and J. H. Lee, J. Korean Phys. Soc. **42**, 233 (2003).

[5] J. Kedzierski, D. M. Fried, E. J. Nowak, T. Kanarsky, J. H. Tankin, H. Hanafi, W. Natzle, D. Boyd, Y. Zhang, R. A. Roy, J. Newbury, C. Yu, Q. Yang, P. Saunders, C. P. Willets, A. Johnson, S. P. Cole, H. E. Young, N. Carpenter, D. Rakowski, B. A. Rainey, P. E. Cottrell, M. Ieong and H.-S. Philip Wong, Tech. Dig., International Electron Devices Meeting, (Washington DC, Dec., 2001), p. 437.

[6] C. Lombardi, S. Manzini, A. Saporito and M. Vanzi, IEEE Trans. Computer-Aided Design **7**, 1164 (1988).

[7] G. Masetti, M. Severi and S. Solmi, IEEE Trans. Electron Devices **30**, 764 (1983).

[8] C. T. Sah, T. H. Ning and L. L. Tschopp, Surface Science **32**, 3619 (1973).

[9] M. Sabathil, S. Hackenbuchner, J. A. Majewski, G. Zandler and P. Vogl, J. Comp. Electronics **1**, 81 (2002).

[10] S. D. Cho, H. T. Kim and D. M. Kim, IEEE Trans. Electron Devices **50**, 1148 (2003).

[11] J. P. Park, H. V. Deshpande and J. C. S. Woo, *IEEE International SOI Conference*, (Durango, CO, Oct., 2001), p. 147.

[12] S. H. Jin, Y. J. Park and H. S. Min, J. Korean Phys. Soc. **44**, 87 (2004).