

Influence of Cu as a catalyst on the properties of silicon nanowires synthesized by the vapour–solid–solid mechanism

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Abstract

Unlike typical Au used as a catalyst for the synthesis of silicon nanowires via the vapour–liquid–solid mechanism, Cu has been found to induce a synthesis process governed by the vapour–solid–solid mechanism. Moreover, the temperature window for obtaining high-quality wires with Cu has been found to be relatively smaller than that shown by the Au: from 600 to 650 °C. However, high-resolution transmission electron microscopy analysis reveals significant new properties of the nanowires obtained. They have the peculiarity of successively switching the silicon structure from diamond to the wurtzite phase along the growth direction. This change of the crystalline structure implies that it has an important impact on the transport properties and characteristics of electronic devices. The results will be important for the future integration and application of silicon, where electrical and thermal transport properties play a significant role.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

Silicon nanowires have attracted significant attention in the last few years in both fundamental and applied studies. On a fundamental side, the nanoscale dimensions lead to inherently quantum mechanical effects such as quantum confinement [1, 2], while on the applied side silicon nanowires hold promise for the realization of high-device-density integrated circuits and interconnects compatible with CMOS technology [3, 4].

One of the most common methods for the synthesis of nanowires is the vapour–liquid–solid method (VLS), in which a metal seed catalyst is required [5, 6]. In many studies, gold (Au) is used as a catalyst, though gold is known to be

a deep-level impurity in silicon [7]. The optical and electronic properties of the nanowires could be improved much further and novel high-level applications realized if alternative metal catalysts or, even better, if no catalyst were used. Additionally, due to cross-contamination issues, the utilization of gold is nowadays incompatible with CMOS technology. The search for new catalysts is therefore crucial for letting the nanowires enter the field of low-dimensional semiconductor structures, future CMOS technology, and nano-optoelectronic devices. It is therefore very important to understand the synthesis of silicon nanowires in systems alternative to the Au–Si system. Aluminium would also constitute an optional material to Au. Indeed, it has already been shown that high-quality silicon nanowires can be synthesized with this metal [8].

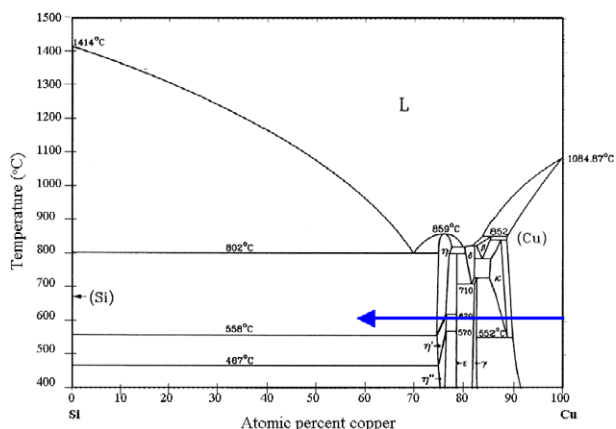


Figure 1. Temperature–composition binary phase diagram of the Cu–Si system.

However, Al oxidizes very rapidly with the presence of traces of oxygen in the environment, meaning that successful implementation requires ultra-high-vacuum conditions, which are usually very costly. On the other side, Cu is currently being used for the interconnects in ICs, and Cu diffusion barriers are standard in technology nowadays. The synthesis of silicon nanowires with Cu as a catalyst could open the way towards the simultaneous fabrication of interconnects and nanowire transistors. Moreover, an understanding of the growth mechanisms of nanowires with other metal catalysts will contribute to a more general understanding of the process, which will guide future synthesis of nanowires with alternative catalysts.

In this paper, we highlight the properties and characteristics of the morphology and structure of silicon nanowires obtained with Cu as a catalyst. The paper is structured as follows. The experimental details are presented in section 2. The experimental results and discussion are presented in section 3, which is divided into five subsections. First, the Cu–Si phase diagram is discussed in relation to the vapour–liquid–solid and vapour–solid–solid mechanisms section 3.1. The temperature window process for obtaining nanowires is then presented and interpreted in section 3.2. The temperature-dependent morphology measured by scanning electron microscopy is shown in section 3.3 and followed by the results concerning the structure of the wires characterized by transmission electron microscopy (section 3.4). Finally, a complementary analysis of the structure by electron energy loss spectroscopy is presented in section 3.5. In section 4 the paper is summarized and concluded.

2. Experimental details

Silicon nanowires were synthesized by catalytic chemical vapour deposition (CVD). Thermally oxidized silicon wafers (with an oxide thickness of $1\ \mu\text{m}$) covered with a 3 nm Cu layer were used as substrates. The Cu layer was obtained by the thermal evaporation of 0.1 mm wires. Once diced into $\sim 2 \times 2\ \text{cm}^2$ pieces, the sample pieces were heated under vacuum and under a flow of 100 sccm of H_2 for 5 min prior to deposition for the sake of getting a uniform temperature through the substrate. For silicon nanowire synthesis, 2.5% of silane was

added to the hydrogen flow. Silane is decomposed only at the surface of the metal, thanks to a Cu-mediated catalytic decomposition reaction [9]. Systematic CVD runs were realized with durations varying between 45 s and 15 min at temperatures ranging between 450 and 750 °C. The deposition time and gas mixture could be accurately controlled using flow meters and a gas valve connected in series at the entrance of the furnace. The ratio between the total silane partial pressure, P_{Si} , and the gas temperature T_g was kept constant, according to the ideal gas law ($P_{\text{Si}}V = NRT_g$), resulting in a constant silane density in the gas phase for the entire range of temperatures used in the experiments.

The morphology and structure were characterized by scanning and transmission electron microscopy (SEM, TEM), as well as by high-resolution TEM. For TEM measurements, the wires were mechanically removed from the substrate by sweeping a clean razor blade through the surface of the substrate. In this way, the nanowires (NWs) then remained at the edge of the foil, and were further removed by dropping a hexane droplet onto it and letting it gently precipitate onto a holey carbon microscope grid for TEM observations. For SEM characterization the samples were observed directly on the substrates. Additionally, electron energy loss spectroscopy measurements were also realized to determine the chemical composition in different locations of the wires.

3. Results and discussion

3.1. Considerations of the Cu–Si thermodynamic diagram and the synthesis of nanowires

A consideration of the Cu–Si phase diagram is helpful for an understanding of the use of Cu as a catalyst for the synthesis of silicon nanowires. The phase diagram concerns mainly the Cu–Si droplet in both the nucleation and steady-state growth stages. In the nucleation stage the silicon alloys with the Cu, prior to precipitation in the form of nanowires, undergoing several structural transformations. During steady-state growth, the phase diagram informs us about the phase involved in the continuous precipitation of silicon in the form of the nanowire. The diagram is shown in figure 1, where it is clear that the binary Cu–Si alloy is not a simple eutectic system, as it is for the Au–Si [10]. As evidenced by the high number of Si–Cu phases that exist, the Cu–Si system presents a high level of complexity. The first point to notice is that the temperature range for the coexistence between liquid Cu and solid silicon lies between 802 and 1084 °C, meaning that this would be the temperature range for the growth of nanowires from Cu through the vapour–liquid–solid process. In principle, however, nanowires should also grow through a vapour–solid–solid process (VSS), as has been observed with Si using Al as a catalyst, and with GaAs and InAs using Au as a seed [11, 12]. As indicated by the phase diagram, a VSS process could occur at temperatures lower than 802 °C. Following the arrow in figure 1, silicon would first diffuse through the Cu, forming a Cu–Si solid alloy (instead of a liquid, as happens in the VLS process). If the alloy supersaturates, precipitation of silicon would occur in the form of a nanowire. This VSS process is possible, provided that catalytic decomposition of silane and the diffusion of silicon through the solid catalyst droplet occur

at a similar rate. In figure 1, an arrow has been drawn to follow the composition of a Cu droplet exposed to silicon diffusion. This arrow indicates the phase transformations of the Cu–Si alloy as the silicon content increases, which would be the process that the Cu droplet would follow during the nucleation of nanowires. As silicon diffuses through the Cu droplet, first Cu_5Si (phases ε and γ) is formed. Then, as more silicon diffuses in and its content increases, Cu_3Si starts to form. By further increasing the silicon content of the seed, silicon finally precipitates from Cu_3Si . Depending on the temperature, the final phase from which the nanowires would precipitate would be one of the three different forms of Cu_3Si : η'' , η' or η . A detailed study on the phase transformations occurring in the catalyst droplet prior to nanowire nucleation would give further insight into the dynamic aspects of the phase transformations presented. It is important to note that the three different Cu_3Si solid phases have a distinct crystalline structure, which might have an influence on the final structure and morphology of the precipitates. It should also be noted that the phase diagram applies to bulk Cu–Si alloys in thermodynamic equilibrium, and that certain deviations should be expected for reduced alloy volumes and under dynamic conditions (growth).

3.2. Temperature process window for nanowire synthesis

For determining the temperature dependence, Cu nanodroplets were exposed to silane at temperatures between 450 and 750 °C. Nanowires were obtained at temperatures between 500 and 650 °C. According to the phase diagram presented above, the synthesis of nanowires from Cu in this temperature range is consistent only through the VSS mechanism.

The low-temperature limit of 500 °C could be attributed to the absence of silane decomposition. However, it has been reported that silane decomposes catalytically at the surface of copper through the VSS process at temperatures as low as 230 °C, invalidating this first hypothesis [13]. We believe that the low-temperature limit should rather be attributed to the low value of the diffusion coefficient of silicon through Cu_3Si , in comparison to the decomposition rate of silane on the Cu surface. Indeed, it has recently been shown that the incubation time, defined as the time necessary for the catalyst to reach super-saturation leading to the growth of nanowires, follows the form [14]:

$$\tau \approx \frac{h^2}{(D_{\text{SO}}) \exp(-E_a/KT)} \quad (1)$$

where h is the height of the catalyst nanoparticle, D_{SO} is related to the pre-factor of the diffusion coefficient of silicon through Cu_3Si , and E_a corresponds to its activation energy. The activation energy for the Cu–Si system is 0.98 eV, which means that, for 10 nm catalyst droplets, the incubation times would increase, for example, from 100 to 400 s when decreasing the synthesis temperature from 500 to 450 °C. We propose that the following happens at lower temperatures. As a consequence of the low values of the coefficient of diffusion of silicon through Cu, there is early silicon super-saturation at the surface of the Cu seed prior to reaching the equilibrium in the whole catalyst. A silicon shell is formed, stopping the further decomposition of silane at the surface of the nanoparticle and therefore the nanowire nucleation.

On the other hand, the growth of silicon nanowires at temperatures higher than 650 °C is limited by a different reason. Our SEM measurements indicate that the surface of the substrate is flat after the CVD run and no droplets are formed. We believe that this is due to the diffusion of copper through the SiO_2 . Indeed, diffusion of copper through SiO_2 has an activation energy of 1.82 eV, which is much higher than the activation energy for diffusion of Si through Cu_3Si (0.98 eV) [15]. This means that, in a certain range of temperatures, the diffusion coefficient of silicon through Cu_3Si can be higher than the coefficient of diffusion of Cu through SiO_2 , allowing the nucleation of silicon nanowires. However, the large value of the activation energy also means that there must be a temperature above which the diffusion of Cu through SiO_2 occurs at a higher rate than the diffusion of Si through Cu_3Si . This temperature is situated slightly above 650 °C, and this is the reason for the lack of nanowire synthesis. For the synthesis of nanowires in higher-temperature regimes, Cu diffusion barriers should be used.

3.3. Temperature dependence of the morphology

CVD runs were realized from 450 to 750 °C on Cu-coated silicon oxidized substrates. After the CVD runs, the samples were first observed using SEM. Representative SEM micrographs of the synthesis realized between 500 and 650 °C are presented in figure 2. Figures 2(a)–(d) correspond to a 15 min synthesis (steady-state growth). Figure 2(e) shows the morphology of the substrate at the initial stage of Cu droplet formation and nanowire nucleation, corresponding to a 45 s process at 650 °C. As it appears in the micrographs, the morphology is dramatically dependent on the temperature of synthesis. In general, two features co-exist: worm-like nanostructures and straight nanowires. The worm-like structures are nanowires with a diameter of about 100 nm that seem to have been growing with a continuous kinking. The other nanowires show a completely different morphology. They are thinner and grow straight with very little kinking. Two-dimensional film growth on the substrate has not been observed at any of the temperatures. At 500 °C, the worm-like structures are predominant and very few straight nanowires exist. As the synthesis temperature is increased, the ratio of worm-like nanostructures to nanowires decreases to the extent that at 600 °C they have nearly disappeared. At 650 °C, no worm-like wires were observed. The diameter of the straight nanowires also changes with temperature. At 500 °C and 650 °C, the diameters are respectively about 10 nm and 100 nm. At 650 °C, nanowires exhibit another specific characteristic, which is that they appear significantly tapered. As the decomposition of silane at 650 °C occurs only at the surface of the metal catalyst, the tapering indicates that the copper is being ‘consumed’ during growth, by dissolving into the wires. Tapering could imply dissolution of the Cu into the wires during growth and therefore we have detrimental consequences on the properties of the wires, but, as has already been shown for Au, this could also imply migration of the Cu to neighbouring wire tips [16].

The origin of the worm-like nanowires can be understood in terms of the spatial-velocity hodograph concept, which was first observed in carbon nanotubes. The origin of this

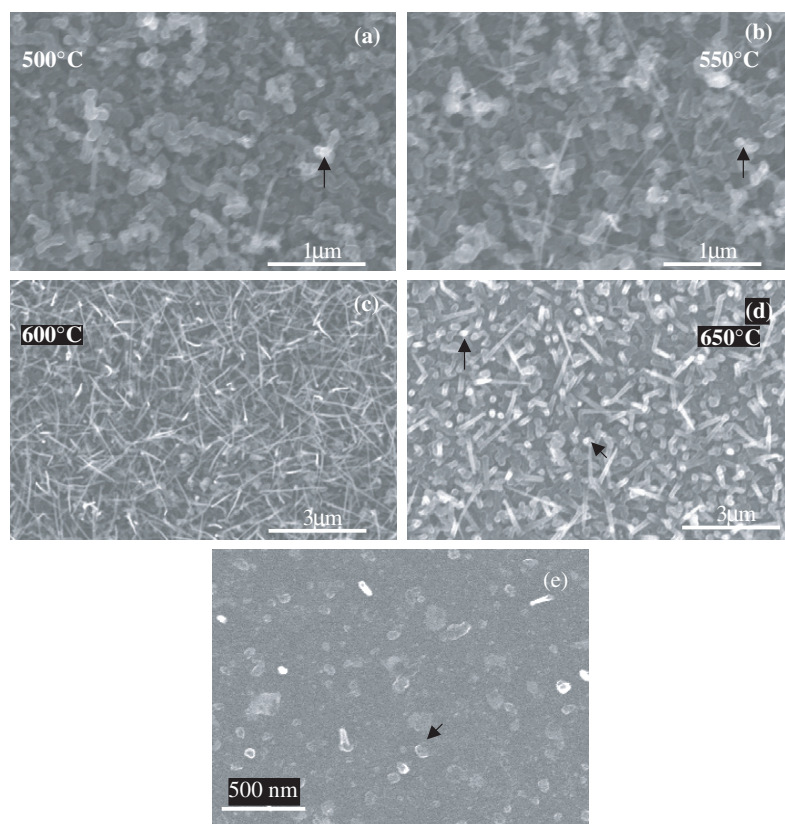


Figure 2. Scanning electron micrographs of 15 min CVD runs realized at temperatures of (a) 500 °C, (b) 550 °C, (c) 600 °C and (d) 650 °C. Two kinds of silicon nanostructures are observed: worm-like (mainly at low temperatures) and straight nanowires (mainly at high temperatures). (e) Scanning electron micrograph of the surface of the substrate after a 45 s CVD run at 650 °C. The initial formation of Cu droplets and some nanowires is observed. Some of the droplets are indicated with an arrow.

phenomenon is the mismatch between the extrusion velocities of silicon within the catalyst because of the different silicon deposition rate along the interface. It has been seen that, under these conditions, this leads to a ‘spontaneous’ plastic deformation of the wire [17]. This effect is especially important at the lowest temperatures, because then the diffusion of silicon through the particle is slower and more inhomogeneous from the border of the nanoparticle to the centre. This effect is also more prominent in the larger wires, as the diffusion of silicon through the whole metal catalyst also takes a longer time and has more chances to be unequal. Following this model, the plastic deformation of the wire should decrease when synthesis is realized at higher temperatures, in agreement with our results.

3.4. TEM and HRTEM measurements

TEM measurements were realized to analyse in detail the structure of the nanowires. Representative TEM micrographs are shown in figure 3. As observed with the SEM, the diameter of the straight nanowires increases with the growth temperature, and consequently it is the largest for synthesis realized at 650 °C. Interestingly enough, the straight nanowires synthesized between 500 and 550 °C seem to be single crystalline and have very few structural defects. No changes in contrast along NWs are observed and no kinking is present on the borders. In contrast, we observe a change in the

growth regime for temperatures equal to or higher than 600 °C, in which the straight nanowires start to grow with defects. Specifically, nanowires synthesized at 600 °C present some regions of contrast modulation along the growth direction, as pointed out by some black arrows in figure 3(c), denoting the presence of structural defects.

At 650 °C, all NWs present a modulated contrast. Measurements with a higher resolution allow us to investigate the nature of this effect closely. HRTEM measurements of wires grown at higher temperature are presented in figure 3(d). There, it is clear that changes in contrast are due a disc-section polycrystalline nature of the nanowires along the growth direction. In order to investigate the nature and origin of this phenomenon further, a more detailed HRTEM study has been undertaken.

The HRTEM micrograph shown in figure 4(a) is representative of the nanowires grown at the highest temperatures—between 600 and 650 °C. In this measurement, the orientation of the wire with respect to the electron beam is such that several families of planes can be observed. The particular orientation of the wire on a highly symmetric zone axis allows the indexing of the lattice planes and correspondence to the crystalline structure [18–20]. In the figure, two grain boundaries determined by stacking faults (SF) are present and are indicated by dashed lines. Both stacking faults are delimiting a twin segment, which in this case is composed of 38 monolayers [21]. A magnification

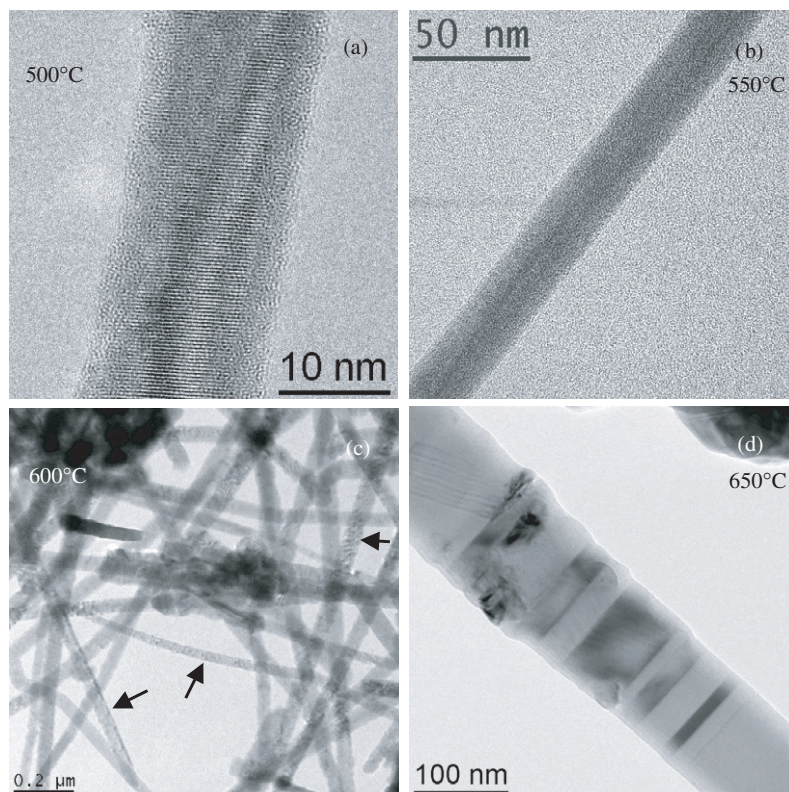


Figure 3. TEM micrographs showing the characteristic morphology of the synthesized Si nanowires at different temperatures. (a) and (b) Micrographs corresponding to the lowest growth temperatures (500 and 550 °C) where silicon nanowires do not present structural defects. (c) TEM micrograph corresponding to the NWs grown at 600 °C. At this temperature some of the wires start showing structural defects (NWs pointed with black arrows). (d) Typical structural morphology of a NW grown at 650 °C. Grain boundaries are present all along the NW.

of the interface is shown in figure 4(b). The crystallographic analysis shows that the regions separated by the stacking faults have a different crystallographic structure. Figure 4(c) corresponds to the power spectrum (fast Fourier transform) of the squared region in figure 4(b). After indexing the power spectra for both regions, we realize that above the boundary the wire crystallizes in the Si IV wurtzite structure, while the structure found below the boundary is the diamond Si I. Si IV and Si I structures have indeed already been observed previously in silicon nanowires synthesized by CVD using gold as a catalyst, but the coexistence of phases within a Si wire is a new phenomenon intrinsic to the use of Cu as a catalyst [22]. The alternation of wurtzite and diamond (zinc-blende in the case of binary compounds) is a novel observation in the case of Si nanowires, but it has been reported recently in the case of GaAs nanowires [20, 23]. As a conclusion, the dark and bright contrast regions in low-resolution TEM can be attributed to different diffraction contrast. The structure of the wires appears stressed, showing cell parameters that differ slightly from the Si IV theoretical structure, as indicated in table 1 [24]. The indexing parameters for the diamond structure corresponding to the power spectrum in figure 4(d) are shown in table 2. We have consistently observed that the cross-sections of Si I and Si IV nanowires alternate along the growth direction with the following epitaxial relationship: $(1\bar{1}1)[110]_{\text{Si I}} \parallel (0002)[1\bar{2}10]_{\text{Si IV}}$, where $(1\bar{1}1)_{\text{Si I}}$ and $(0002)_{\text{Si IV}}$ are the growth planes for every phase, both with an inter-planar

distance of 0.313 nm. Interesting enough is that the epitaxial relationship that is found coincided with the one found on the GaAs wurtzite/zinc-blende alternating heterostructures in GaAs NWs [20]. The epitaxial relationship between Si I and Si IV occurs by a double twinning mechanism, which was also reported by Pirouz *et al* on bulk silicon samples which were submitted to high pressures [25–27]. The origin of the switching of structure is not yet understood, and should be investigated further in the future. One hypothesis would be the mismatch between the wire and the catalyst, which consists by a solid alloy of Si and Cu. This mismatch would be more important for the case of thick wires, as the stress energy is larger and thus more difficult to accommodate [28].

3.5. EELS profiles in scanning TEM (STEM) mode

In order to confirm further that the contrast in the TEM measurements is not due to changes in the chemical composition, electron energy loss spectroscopy (EELS) was realized at different points along the growth direction of the wires. In figure 5(a), a bright-field scanning TEM (BF STEM) micrograph of a wire presenting several of these strong contrast modulations is presented. The regions indicated by letters on the wire correspond to different regions analysed using EELS with nanometre resolution. The corresponding energy loss near edge spectra (ELNES) obtained at the L-edge of silicon (99 eV) are shown in figure 5(b). The spectra obtained in the different regions are similar with no changes, indicating that there is no appreciable change in silicon atomic bonds at the

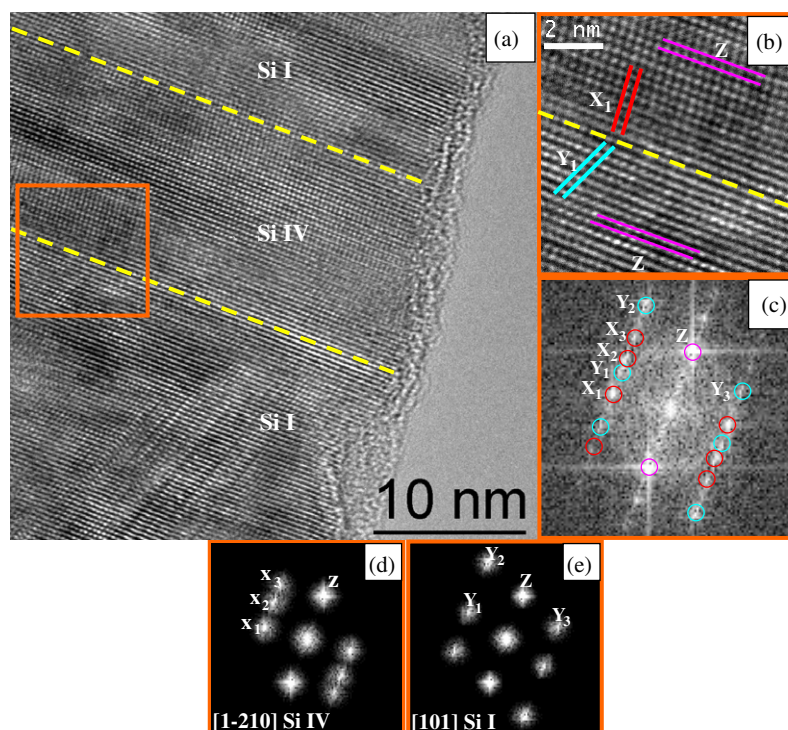


Figure 4. (a) High-resolution transmission electron micrograph of a straight nanowire synthesized at 600 °C. The dashed lines indicate the stacking fault (SF) position delimiting the silicon wurtzite/diamond heterostructure. (b) A close-up of the squared region in (a). (c) Indexed power spectrum of the same region showed in (b). Notice that the spectrum has been taken on the phase boundary. (d) Mask applied to the spots corresponding to the upper region (A), which corresponds to wurtzite silicon (Si IV). (e) Mask applied to the spots corresponding to the bottom region (B), which corresponds to diamond silicon (Si I).

Table 1. Indexing results obtained from the power spectra presented in figure 4(d).

Figure 4(d) spot #	d (nm) experimental	(°) versus spot Z experimental	Indexation proposed	d (nm) theoretical	(°) versus spot Z theoretical
Z	0.313	—	(0002)	0.313	—
X ₁	0.294	65	(10 $\bar{1}$ 1)	0.291	62
X ₂	0.327	86	(10 $\bar{1}$ 0)	0.329	90
X ₃	0.242	48	(10 $\bar{1}$ 2)	0.227	44

Zone axis: $[1\bar{2}10]$ Si IV

Table 2. Indexing results obtained from the power spectra presented in figure 4(e).

Figure 4(e) spot #	d (nm) experimental	(°) versus spot Z experimental	Indexation proposed	d (nm) theoretical	(°) versus spot Z theoretical
Z	0.313	—	(1 $\bar{1}$ 1)	0.313	—
Y ₁	0.320	71	(1 $\bar{1}$ 1)	0.313	71
Y ₂	0.191	35	(2 $\bar{2}$ 0)	0.192	35
Y ₃	0.274	56	(002)	0.271	55

Zone axis: $[110]$ Si I

different wire positions. These results are in good agreement with those shown by Pirouz *et al*, as no noticeable difference between Si I and Si IV spectra is found since, in both cases, the silicon atoms are bound in a tetrahedral configuration. Indeed, the only difference between the structures lies in the order of the tetrahedra, and this leads to equivalent EELS and ELNES responses. Additionally, we would like to point out

that no signal of Cu was found in EELS spectra measured at the same points. We therefore conclude that the contrast modulation along the wires in the TEM measurements is due to a change in the silicon crystal structure during growth, as HRTEM micrographs certify. The structural modulation along the growth direction will have a strong impact on the electronic transport properties of the wires. The mechanisms

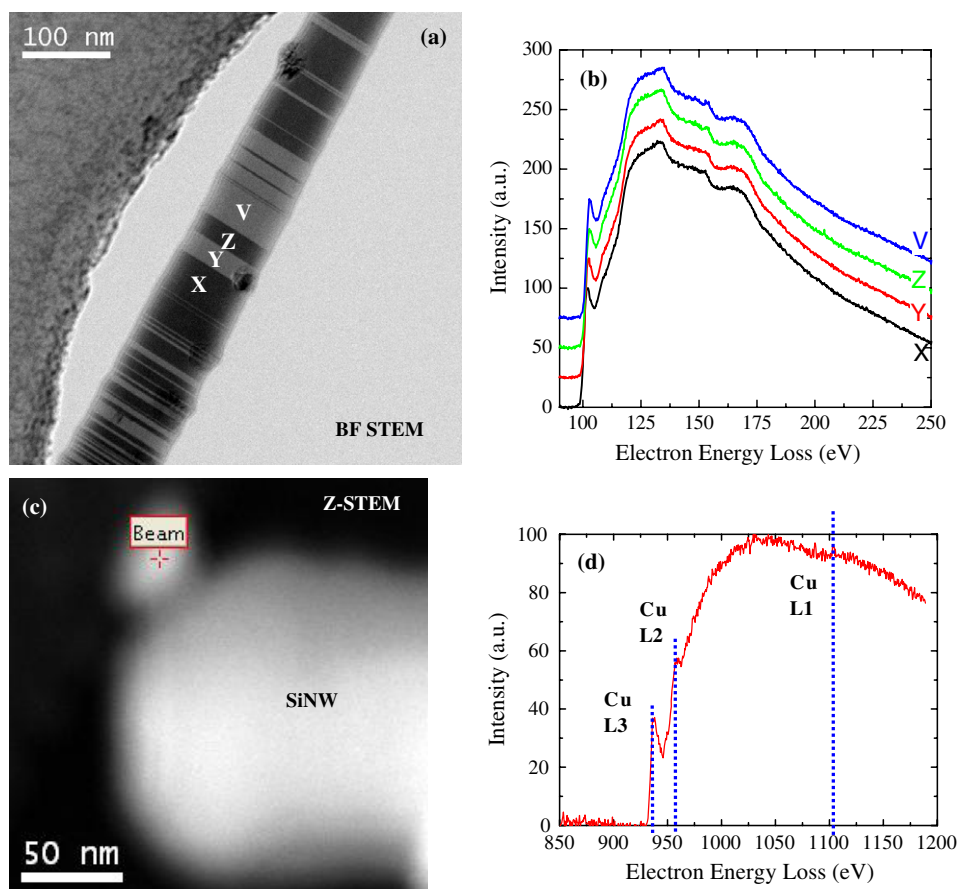


Figure 5. (a) Bright-field scanning TEM micrograph of a nanowire presenting numerous contrast zones. (b) Electron energy loss spectra of zones of the wire with different contrast. The spectra have been shifted vertically for better clarity. (c) Z contrast scanning transmission electron micrograph of the tip of a nanowire. The tip of the nanowire is indicated by a cross for chemical analysis. (d) Electron energy loss spectra of the region at the tip of the nanowire, indicated in (c).

involved in such structural modulation need to be investigated further in the future. In figure 5(c), a TEM measurement of the tip of a silicon nanowire synthesized at 650 °C is shown. The Cu nanoparticle appears smaller than the diameter, in agreement with the tapering observed in the SEM micrographs. The composition of the nanoparticle has been analysed. The corresponding EELS spectrum is shown in figure 5(d). The L2 and L3 edges of the Cu have been measured at 936 and 958 eV, respectively, indicating the presence of Cu, as expected.

4. Summary and conclusions

Summarizing, we have shown that the synthesis of silicon nanowires with Cu as a catalyst occurs via the vapour–solid–solid process. The morphology of the wires depends strongly on temperature, with the window between 600 and 650 °C being optimal with regard to the structural properties of the wires. Additionally, we have shown that the structure of the wires changes continuously along the growth direction from diamond to wurtzite (both being semiconductor Si phases), which should have an important impact on the electrical and thermal transport properties of the wires and therefore affect their future implementation in electronic applications. These results will be important for the integration of silicon nanowires and Cu interconnects.

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